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EXAMINER	
QUINTO, KEVIN V	

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2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,294	TU ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-25 and 27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,12,13,19 and 20* is/are allowed.

6)☒ Claim(s) *1-6,9-11,15-18, 21-25, and 27-30* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed September 7, 2006 have been fully considered but they are not persuasive. The arguments concerning claims 1–13, 15-25, and 27-30 appear to be based on the reasoning that Jin et al. (United States Patent Application Publication No. US 2003/0183862 A1) does not disclose a "recessed region" with a conductive layer that couples two adjacent capacitors. The applicant's currently filed specification describes a "recessed region" in the structures shown in figures 2M, 4M, 3M, 6, 7, and 8. The "recessed region" of an insulating layer (240 for figure 4M, 362 for figure 6, and 472 for figure 8) contains "a connecting region" (265 for figure 4M, 365 for figure 6, and 465 for figure 8) which couples two capacitors together. The term "recessed" describes the relationship between the top of the conductive layer (262 for figure 4M, 384 for figure 6, 484 for figure 8) and the top of the insulating layer (240 for figure 4M, 362 for figure 6, and 472 for figure 8). This relationship is clearly shown in the Jin structures of figures 10H and 11B. The insulating layer (220 or 224 or 230 or 232 or 234) is recessed from the connecting region (242) which couples two capacitors together. Therefore the limitation of "recessed region" fails to patentably distinguish over the Jin structure of figures 10H and 11B because this limitation is met.

Claim Objections

2. Claim 15 is objected to because of the following informalities: the phrase "plurality of MIM capacitor" in line 5 of the claim is grammatically incorrect. Appropriate correction is required.

3. Claim 18 is objected to because of the following informalities: the word *at* is misspelled as "st" in line 1 of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 30 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a first insulating layer, does not reasonably provide enablement for a first insulating layer having at least one first insulating layer and a conductive region which form a first metallization layer. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make or use the invention commensurate in scope with these claims.

6. Claim 30 states that the "conductive region and the at least first insulating layer comprise at least one first metallization layer of the semiconductor device." However claim 30 is dependent upon claim 29 which already describes the conductive region as being in the second insulating layer which is between the workpiece and the first

insulating layer. The examiner is unable to find an embodiment within the currently filed specification which supports claim 30.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-6, 9-11, 15-18, 22-25, and 27-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Jin et al. (United States Patent Application Publication No. US 2003/0183862 A1).

9. In reference to claim 1, Jin et al. (United States Patent Application Publication No. US 2003/0183862 A1, hereinafter referred to as the "Jin" reference) discloses a device which meets the claim. Figures 10H and 11B of Jin each illustrates a semiconductor device with a first insulating layer (218) formed over a workpiece (not shown). There is at least one second insulating layer (220 or 224 or 230 or 232 or 234) formed over the first insulating layer (218). At least one metal-insulator-metal (MIM) capacitor of a plurality of MIM capacitors is formed in the first insulating layer (218) and the at least one second insulating layer (220 or 224 or 230 or 232 or 234). The at least one MIM capacitor has a first conductive layer (238), a dielectric layer (240) disposed

over the first conductive layer (238), and a second conductive layer (242) formed over the dielectric layer (240). The first conductive layer (238) extends completely to a top surface of the at least one second insulating layer (220 or 224 or 230 or 232 or 234). The at least one second insulating layer (220 or 224 or 230 or 232 or 234) comprises a recessed region between at least two adjacent MIM capacitors. The least two adjacent MIM capacitors comprise a top plate comprised of the second conductive layer (242). The second conductive layer (242) within the recessed region electrically couples together the top plates of at the least two adjacent MIM capacitors.

10. With regard to claim 2, the first conductive layer (238) and the second conductive layer (242) comprise refractory metals and nitrides of these metals which meet the claim (p. 8, paragraph 136).

11. With regard to claim 3, the dielectric layer (240) is formed of several materials which meet the claim (p. 8, paragraph 137).

12. In reference to claim 4, the at least one second insulating layer (220 or 224 or 230 or 232 or 234) comprises five or more insulating layers in which the MIM capacitor is formed in its entirety.

13. With regard to claim 5, the workpiece comprises a plurality of elements formed therein (p. 7, paragraph 125). A third insulating layer (210) is formed between the workpiece and the first insulating layer (218). There is at least one first conductive region (212, 214a) disposed in the third insulating layer (210) abutting the first conductive layer (238) of the at least one of the plurality of MIM capacitors, wherein the at least one first conductive region (212, 214a) and the first conductive layer (238)

comprise a bottom plate of the at least one of the plurality of MIM capacitors. Furthermore it is understood that the first conductive region (212, 214a) couples the at least one MIM capacitor to an element on the workpiece.

14. In reference to claim 6, the third insulating layer (210) comprises a first metallization layer of the semiconductor device (p. 7, paragraph 125). The first insulating layer (218) comprises a first via layer of the semiconductor device, wherein the second insulating layer (220 or 224 or 230 or 232 or 234) comprises a second metallization layer of the semiconductor device. The at least one of the plurality of MIM capacitors is formed in the first via layer (218) and the second insulating layer (220 or 224 or 230 or 232 or 234) of the semiconductor device.

15. In reference to claim 9, the first conductive layer (238) comprises a bottom electrode, the dielectric layer (240) comprises a capacitor dielectric, and the second conductive layer (242) comprises a top electrode. The examiner notes the limitation with regard to the use of a chemical-mechanical polish (CMP) process to form the top and bottom electrodes. However this places claim 9 into the form of a **product-by-process claim**:

> Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe,* 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161*; In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi* et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claim 9 does not distinguish over the Jin reference regardless of the process used to form the top and bottom electrodes, because only the final product is relevant, and not the process of making such as chemical-mechanical polishing (CMP).

16. With regard to claim 10, Jin discloses that the capacitors are intended for use in a mixed-mode device (p. 1, paragraph 2).

17. In reference to claim 11, the workpiece comprises a first region and a second region, wherein the MIM capacitors are formed over the first region, further comprising conductive regions (228 – both figures 10H and 11B, and although not shown to completion; the opening (250) in figure 10B) formed in the first insulating layer (218) and the second insulating layer (220 or 224 or 230 or 232 or 234) over the second region of the workpiece.

18. In reference to claims 15 and 17, the workpiece comprises a plurality of elements formed therein (p. 7, paragraph 125). A third insulating layer (210) is formed between the workpiece and the first insulating layer (218), further comprising at least one first conductive region (212, 214a) disposed in the third insulating layer (210) abutting the first conductive layer (238) of the at least one of the plurality of MIM capacitors, wherein the at least one first conductive region (212, 214a) and the first conductive layer (238) comprise a bottom plate of the at least one of the plurality of MIM capacitors. Furthermore it is understood that the first conductive region (212, 214a) couples the at least one of the plurality of MIM capacitors to an element on the workpiece.

19. With regard to claim 16, the at least one first conductive region (212, 214a) comprises a conductive barrier layer (212) and a conductive material (214a) disposed over the conductive barrier layer (212).

20. In reference to claim 18, the first conductive region (212, 214a) and the third insulating layer (210) comprise a first metallization layer of the semiconductor device (p. 7, paragraph 125). The first insulating layer (218) comprises a first via layer of the semiconductor device, wherein the second insulating layer (220 or 224 or 230 or 232 or 234) comprises a second metallization layer of the semiconductor device. The at least one of the plurality of MIM capacitors is formed in the first via layer (218) and the second metallization layer (220 or 224 or 230 or 232 or 234) of the semiconductor device.

21. In reference to claim 22, Jin (United States Patent Application Publication No. US 2003/0183862 A1) discloses a device which meets the claim. Figures 10H and 11B of Jin each illustrates a semiconductor device with a first insulating layer (218) formed over a workpiece (not shown). There is at least one second insulating layer (224) formed over the first insulating layer (218). There is at least one third insulating layer (232) formed over the second insulating layer (224). At least one metal-insulator-metal (MIM) capacitor is formed in the first insulating layer (218), the second insulating layer (224), and the third insulating layer (232). The at least one MIM capacitor has a first conductive layer (238), a dielectric layer (240) disposed over the first conductive layer (238), and a second conductive layer (242) formed over the dielectric layer (240). The at least one third insulating layer (232) comprises a recessed region between at least

two adjacent MIM capacitors. The least two adjacent MIM capacitors comprise a top plate comprised of the second conductive layer (242). The second conductive layer (242) within the recessed region electrically couples together the top plates of at the least two adjacent MIM capacitors.

22. In reference to claim 23, the first insulating layer (218) comprises a first via layer of the semiconductor device, wherein the second insulating layer (224) comprises a first metallization layer of the semiconductor device. The third insulating layer (232 in figure 10H) comprises at least one second via layer and at least one second metallization layer of the semiconductor device. The at least one of the plurality of MIM capacitors extends through the entire thicknesses of the first via layer (218), the first metallization layer, the at least one second via layer, and the at least one second metallization layer.

23. With regard to claim 24, the workpiece comprises a plurality of elements formed therein (p. 7, paragraph 125). A fourth insulating layer (210) is formed between the workpiece and the first insulating layer (218). There is at least one first conductive region (212, 214a) disposed in the fourth insulating layer (210) between the first conductive layer (238) of the at least one of the plurality of MIM capacitors and an element in the workpiece. Furthermore it is understood that the first conductive region (212, 214a) couples the at least one of the plurality of MIM capacitors to an element on the workpiece. The at least one first conductive region (212, 214a) and the first conductive layer (238) comprise a bottom plate of the at least one of the plurality of MIM capacitors.

24. In reference to claim 25, the fourth insulating layer (210) comprises a first metallization layer of the semiconductor device (p. 7, paragraph 125). The first insulating layer (218) comprises a first via layer of the semiconductor device, wherein the second insulating layer (224) comprises a second metallization layer of the semiconductor device. The at least one third insulating layer (232 – see figure 10H) comprises at least one second via layer and at least one third metallization layer. The at least one of the plurality of MIM capacitors extends through the entire thicknesses of the first via layer (218), the first metallization layer, the at least one second via layer, and the at least one second metallization layer.

25. In reference to claim 27, Jin (United States Patent Application Publication No. US 2003/0183862 A1) discloses a device which meets the claim. Figures 10H and 11B of Jin each illustrates a semiconductor device with a first insulating layer (218, 224) formed over a workpiece (not shown). There is a plurality of metal-insulator-metal (MIM) capacitors is formed in the at least one first insulating layer (218). The plurality of MIM capacitors has a first conductive layer (238), a dielectric layer (240) disposed over the first conductive layer (238), and a second conductive layer (242) formed over the dielectric layer (240). The second conductive layer (242) comprises a top plate of the plurality of MIM capacitors. A top of the least one first insulating layer (218, 224) comprises a recessed region between at least two adjacent MIM capacitors. The second conductive layer fills the recessed region of top of the first insulating layer (218, 224), electrically coupling together the top plates of at the least two adjacent MIM capacitors.

26. With regard to claim 28, the at least first insulating layer (218, 224) comprises at least two insulating layers. One first insulating layer (218) comprises a via layer of the semiconductor device while the other first insulating layer (224) comprises an interconnect layer formed over the via layer.

27. In reference to claim 29, the workpiece comprises a plurality of elements formed therein (p. 7, paragraph 125). At least one second insulating layer (210) is formed between the workpiece and the first insulating layer (218, 224). A conductive region (212, 214a) is formed in each of the least one second insulating layer (210) and is electrically coupled to the first conductive layer (238) of the MIM capacitors. The conductive region (212, 214a) and the first conductive layer (238) comprise a bottom plate of the at least one MIM capacitor. Furthermore it is understood that the conductive region (212, 214a) couples the MIM capacitors to an element on the workpiece.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. (United States Patent Application Publication No. US 2003/0183862 A1) in view of Yang et al. (USPN 6,417,537 B1).

30. With regard to claim 21, Jin discloses the use of a conductive material for the second conductive layer or top electrode of the at least one of the plurality of MIM capacitors but does not disclose the use of a conductive layer comprising a conductive barrier layer and a conductive material disposed over the conductive barrier layer. However the use of such an electrode structure is well known the art. Yang (USPN 6,417,537 B1) discloses a top electrode capacitor structure formed of a conductive material (265) which is disposed over a conductive barrier layer (260) in figure 2I. Yang discloses that such an electrode structure protects the top electrode from oxidation (column 10, lines 42-67) which is a known problem in the art (column 2, lines 12-20). In view of Yang, it would therefore be obvious to implement a top electrode for capacitor which is formed of a conductive material that is disposed over a conductive barrier layer in the device of Jin.

Allowable Subject Matter

31. Claims 7, 12, 13, 19, and 20 are allowed.

32. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

33. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a semiconductor device with a metal-insulator-metal capacitor having the explicit bottom plate electrode and interlevel dielectric layer structures as suggested by the applicant.

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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KVQ

EVAN PERT
PRIMARY EXAMINER